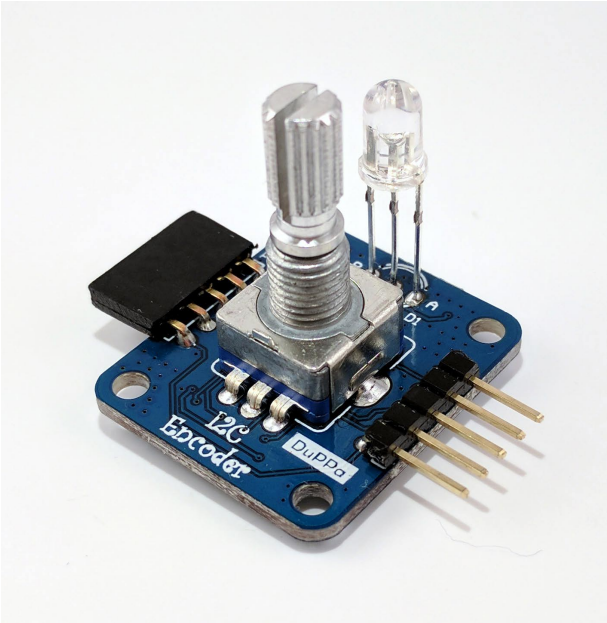


I2C Encoder

HW v1.2

Revision History

Revision	Date	Author(s)	Description
1.0	22.11.17	Simone	Initial version

Contents

1. Device Overview

The I2C Encoder is a small board where you can use a classical mechanical encoder with a I^{2}C bus. The device include also the possibility to add a bi-color LED and set luminosity trough the I^{2}C bus. It's possible to connect up to 16 boards in cascade and read all of them with the same I^{2}C bus.

The I2C Encoder have a series of 8 bit register where it is possible to configure the parameters and three 32 bit of register. The 32 bit registers are the most important because they store the counter value and the maximum and minimum threshold. Every time when the encoder is moved at least one step, the counter value is increased or decreased according to the rotation direction. When the counter value is outside of the limit set by the threshold, the counter value can be wrapped or can stuck on the threshold valued reached.

The I2C Encoder also has an open-drain interrupt pin. It is set to logic low every time when the encoder is rotated or pushed. The status register must be read by the master to check what is changed.

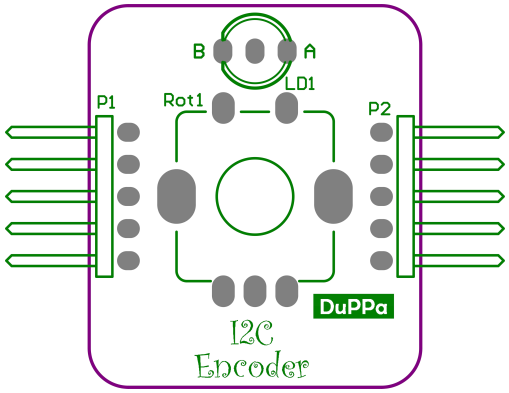


Figure 1.1: Top view of the board

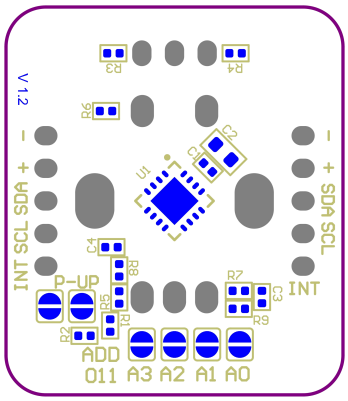


Figure 1.2: Bottom view of the board

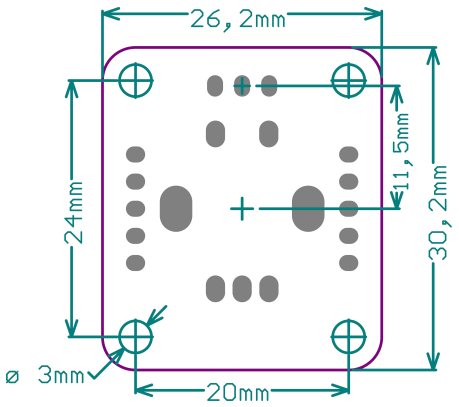


Figure 1.3: Dimensions of the board

1.1 Electrical characteristics

Parameter	Symbol	Min	Max
Supply voltage	V_{DD}	2.5V	5V
I^2C input-low level	V_{IL}	0	0.3 * V_{DD}
I^2C input-high level	V_{IH}	0.8 * V_{DD}	V_{DD}
I^2C clock input frequency	f_{SCL}		400kHz
LED output current	I_{LED}		30mA
Supply current (LEDs off)	I_{DD}		1.8mA
I^2C pull-up resistor	R_{I^2C}		4.7kΩ
Interrupt pull-up resistor	R_{INT}	15kΩ	120kΩ

1.2 Connection

Figure 1.4 shows the pin out of the I2C Encoder.

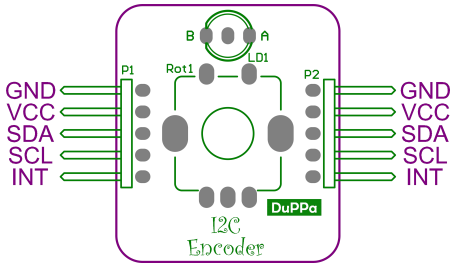


Figure 1.4: Pin-out of the board

Pin	I/O Type	Function
GND	Power	Ground reference for logic
Vcc	Power	Positive supply for logic
SDA	I/O	I^2C data
SCL	I	I^2C clock
INT	OD	Open-drain interrupt output

There are two 5 pin headers one the right and one at the left side of the I2C Encoder. The I2C Encoder can be connected in cascade as showed in figure 1.5, the maxim number of device is 16 due to the limitation of the I^2C address. Since the INT pin is open drain, the signal is propagated along the chain in case of interrupt of one device. In order to avoid I^2C address conflict, the address of each device must be different. In the section 1.3, it is described how to set the address.

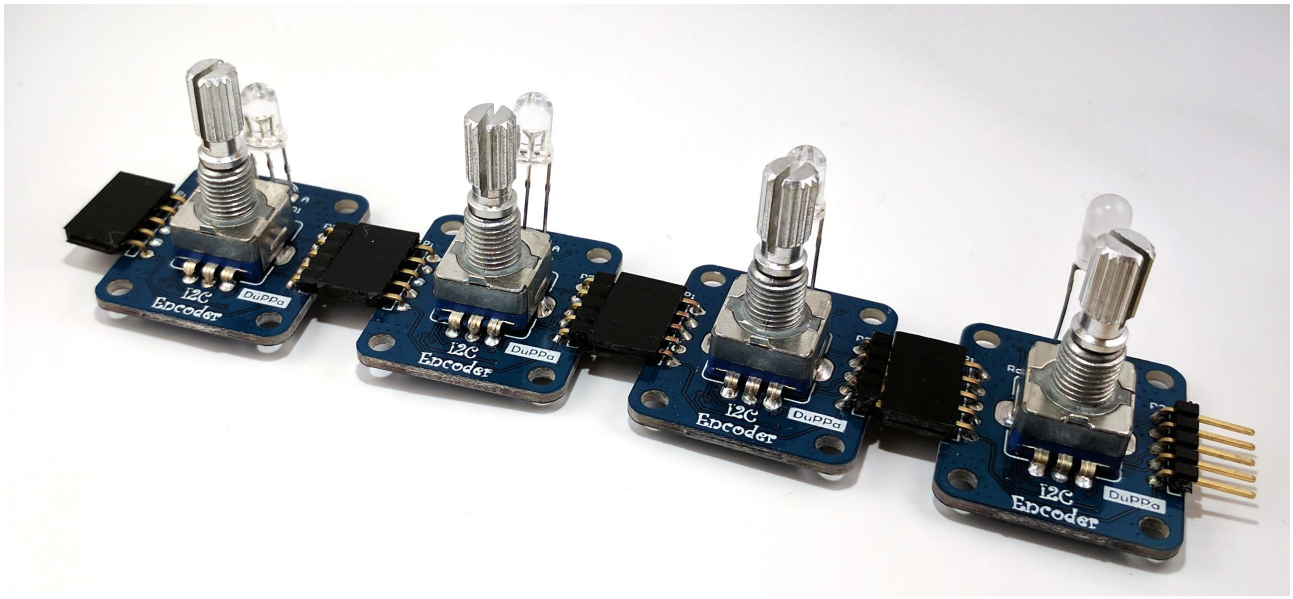


Figure 1.5: Example of 4 boards connected in cascade

1.3 I²C interface

The I2C Encoder is a I²C slave, it's possible to the set 16 different addresses. The last four LSB of the 7-bit address can be customized by soldering the jumpers A0 - A3 on the bottom of the board. When the jumper is open, it means a logic 0. if jumper is shorted it means a logic 1.

I²C address							
7	6	5	4	3	2	1	0
0	1	1	A3	A2	A1	A0	R/W

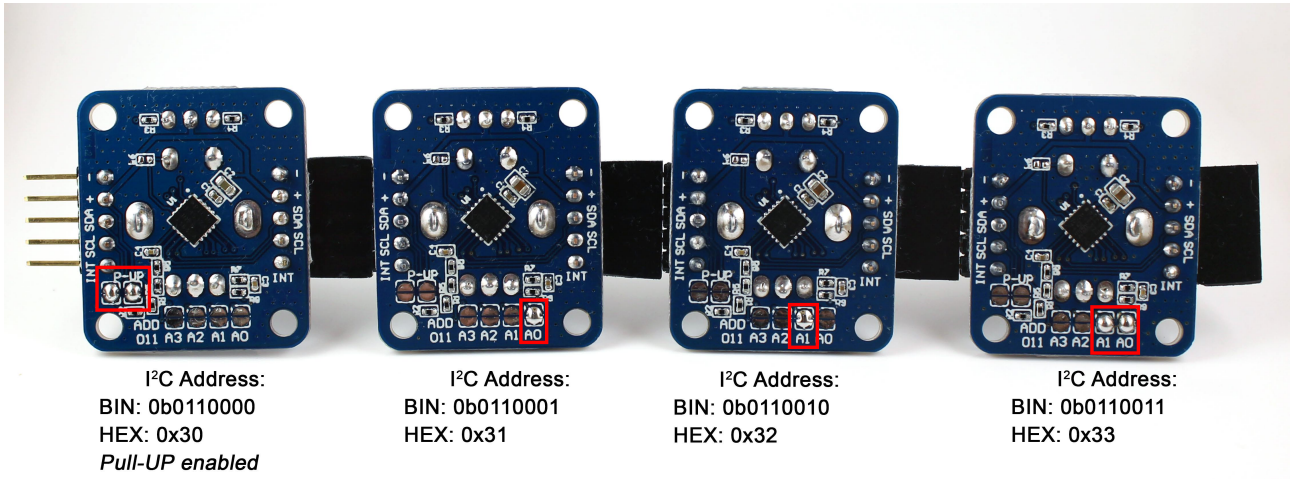


Figure 1.6: Example of the address setting of the board in figure 1.5

The I2C Encoder has the I²C pull-up resistors. They can be enabled by soldering the two jumpers **P-UP** like in the figure 1.6. This must be done in case that the master doesn't have these resistors and must be enabled only one I2C Encoder in a chain.

In case the pull-up resistors is not needed, the jumpers **P-UP** must be removed.

2. Registers

In this section, the internal registers of I2C Encoder is described.

Address	Description	Default value
0x00	General Configuration	0x00
0x01	Status	0x00
0x02	Counter Value Byte 4	0x00
0x03	Counter Value Byte 3	0x00
0x04	Counter Value Byte 2	0x00
0x05	Counter Value Byte 1	0x00
0x06	Counter Max Byte 4	0x00
0x07	Counter Max Byte 3	0x00
0x08	Counter Max Byte 2	0x00
0x09	Counter Max Byte 1	0x00
0x0A	Counter Min Byte 4	0x00
0x0B	Counter Min Byte 3	0x00
0x0C	Counter Min Byte 2	0x00
0x0D	Counter Min Byte 1	0x00
0x0E	LED A intensity	0x00
0x0F	LED B intensity	0x00

2.1 Configuration

2.1.1 General Configuration

Address: **0x00**							
7	6	5	4	3	2	1	0
R/W-0	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
RESET	-	RMOD	IPUD	DIRE	WRAPE	LEDE	INTE

INTE Enable interrupt pin.

1: Enable

0: Disable

LEDE Enable LED output.

1: Enable

0: Disable

WRAPE Enable counter wrap.

1: Wrap enable. When the counter value reaches the **CMAX**+1, restart to the **CMIN** and vice versa

0: Wrap disable. When the counter value reaches the **CMAX** or **CMIN**, the counter stops to increasing or decreasing

DIRE Direction of the encoder when increment.

1: Rotate left side to increase the value counter

0: Rotate right side to increase the value counter

IPUD Interrupt Pull-UP disable.

1: Disable

0: Enable

RMOD Reading Mode.

1: X2 mode

0: X1 mode

RST Reset of the I2C Encoder

1: Reset

0: No reset

2.2 Status

Address: **0x01**							
7	6	5	4	3	2	1	0
-	-	-	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
-	-	-	RMIN	RMAX	RDEC	RINC	PUSH

PUSH Status of the push button of the encoder

1: Push button is pressed

0: Push button is not pressed

RINC Status of the counter value

1: Counter value is increased

0: Counter value is not increased

RDEC Status of the counter value

1: Counter value is decreased

0: Counter value is not decreased

RMAX Status of the counter value

1: **CVAL** reaches the **CMAX** value

0: **CVAL** is below the **CMAX** value

RMIN Status of the counter value

1: **CVAL** reaches the **CMIN** value

0: **CVAL** is above the **CMIN** value

2.3 Counter Value

2.3.1 Counter Value

Address: **0x02**							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 4 <31 - 24>							
Address: **0x03**							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 3 <23 - 16>							
Address: **0x04**							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 2 <15 - 8>							
Address: **0x05**							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CVAL BYTE 1 <7 - 0>							

This is a signed 32 bit register where the counter value is stored. When the encoder is rotated, the value is increased or decreased according to the direction.

2.3.2 Counter Max

Address: **0x06**							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 4 <31 - 24>							
Address: **0x07**							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 3 <23 - 16>							
Address: **0x08**							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 2 <15 - 8>							
Address: **0x09**							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMAX BYTE 1 <7 - 0>							

This is a signed 32 bit register, it is used for storing the maximum threshold of the **CVAL** register. When **CVAL** is greater than **CMAX**, the value of **CVAL** is set according the the flag **WRAPE**.

2.3.3 Counter Min

Address: **0x0A**							
31	30	29	28	27	26	25	24
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 4 <15 - 8>							
Address: **0x0B**							
23	22	21	20	19	18	17	16
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 3 <7 - 0>							
Address: **0x0C**							
15	14	13	12	11	10	9	8
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 2 <15 - 8>							
Address: **0x0D**							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
CMIN BYTE 1 <7 - 0>							

This is a signed 32 bit register, it is used for storing the minimum threshold of the **CVAL** register. When **CVAL** is less than **CMIN**, the value of **CVAL** is set according the the flag **WRAPE**.

2.4 LEDs

2.4.1 LED A intensity

Address: **0x0E**							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LED A PWM Value <7 - 0>							

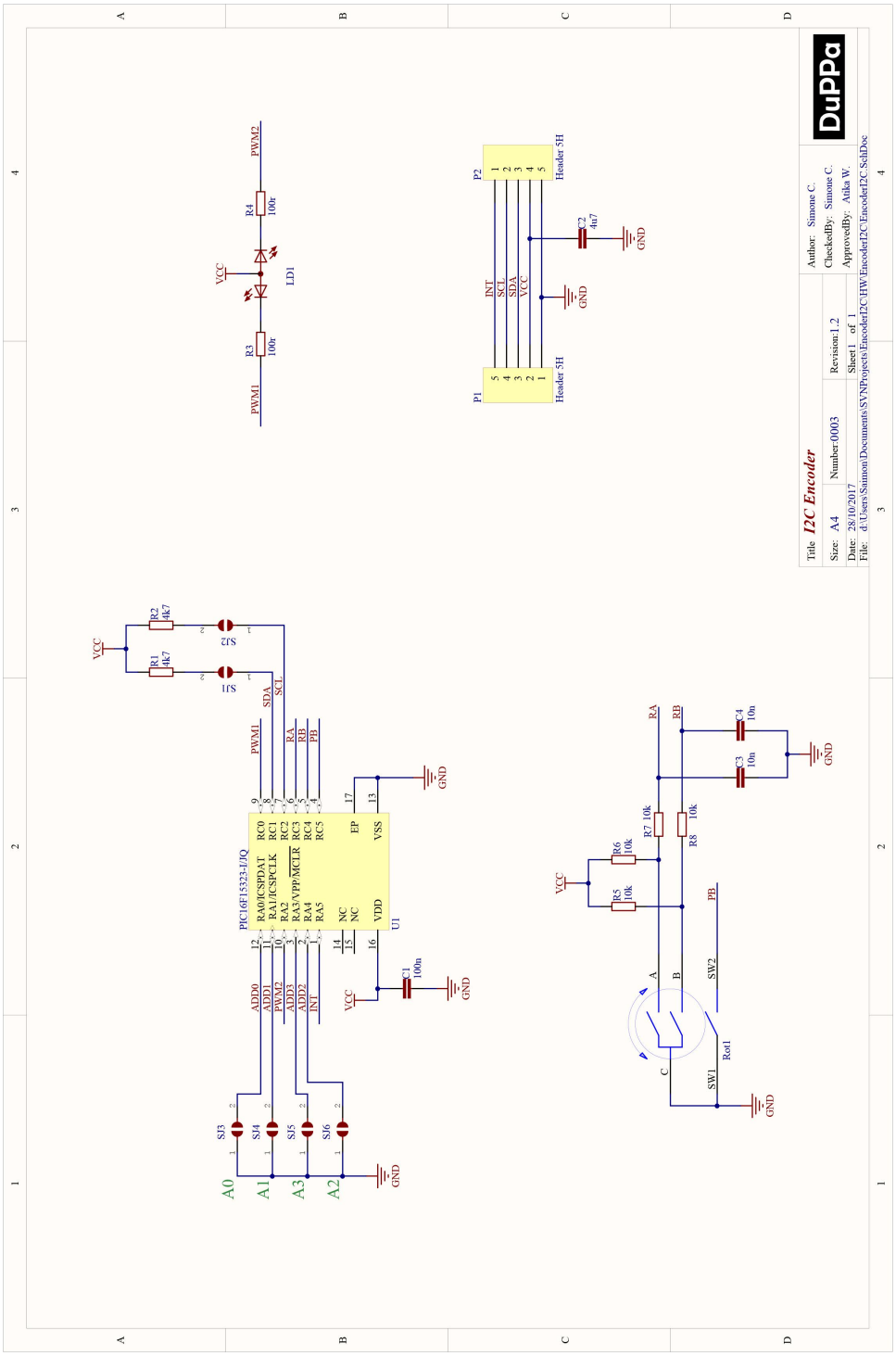
This register is used for setting the PWM of the **LED A**, where the value of **0x00** means PWM at 0% and a value of **0xFF** means PWM at 100%.

2.4.2 LED B intensity

Address: **0x0F**							
7	6	5	4	3	2	1	0
R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0	R/W-0
LED B PWM Value <7 - 0>							

This register is used for setting the PWM of the **LED B**. A value of **0x00** means PWM at 0% and a value of **0xFF** means PWM at 100%

3. Schematic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Size: A4
Number:0003
Revision:1.2
Date: 28/10/2017
Sheet 1 of 1
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Author: Simone C.
CheckedBy: Simone C.
ApprovedBy: Atika W.
PIC16F15323-I/JQ
Header 5H
LD1
SW1
SW2
Rot1